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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,474	01/26/2004	Sehat Sutardja	MP0319	9439

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HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 400
TROY, MI 48098

EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,474	SUTARDJA, SEHAT	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44,147,148 and 153* is/are pending in the application.

4a) Of the above claim(s) *45-95,137-146,149,150 and 154* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,24,25,27,37,38,147,148 and 153* is/are rejected.

7)☒ Claim(s) *7,11-23,26,28-36 and 39-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/26/04, 3/7/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species III, comprising claims 1-44, 147, 148 and 153 in the response filed 24 August 2006 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There are no drawings or disclosure of the second and third plane-like metal layers being coplanar. Figure 4C discloses only the second and third plane-like metal layers being in separate, parallel planes.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 2, 4-6, 8-10, 24, 25, 27, 37, 38, 147, 148 and 153 are rejected under 35 U.S.C. 102(e) as being anticipated by Eden et al.. As to claim 1, Eden et al., Figure 7, discloses an integrated circuit, comprising: first (78a), second (74c), and third (76) plane-like metal layers; a first transistor (examiners notation "1st") having a first terminal (S_1) that communicates with said second plane-like metal layer and a second terminal (D_1) that communicates with said first plane-like metal layer; a second transistor (examiners notation "2nd") having a third terminal (S_2) that communicates with said first plane-like metal layer and a fourth terminal (D_2) that communicates with said third plane-like metal layer. Eden et al., Figure 13, discloses that first and second control terminals (164) may be formed for each transistor, and that a fourth plane-like metal layer (Figure 9, element 114a) that includes first, second and third contact portions that communicate with said second plane-like metal layer (110), said first plane-like metal layer (111) and said third plane-like metal layer (112), respectively.

As to claim 2, Eden et al., Figure 9, discloses that the fourth plane-like metal layer is a top layer that is thicker than said first, second and third plane-like metal layers.

As to claim 4, Eden et al., Figure 7, discloses that said second (74c) and third (76) plane-like metal layers are in separate planes.

As to claim 5, Eden et al., Figures 7 and 13, discloses a plurality of local interconnects, comprising solder balls (84a) and control terminals that communicate with said first terminal, said second terminal and said first control terminal of said first transistor and said third terminal, said fourth terminal and said second control terminal of said second transistor.

As to claim 6, Eden et al., paragraph [0083], discloses that the first and second transistors are NMOS transistors, said first and second control terminals are gates (paragraph [0102]), said first and third terminals are drains (Fig. 7, D_1 and D_2) and said second and fourth terminals are sources (Fig. 7, S_1 and S_2).

As to claim 8, Eden et al., Figure 7, discloses that the first plane-like metal layer (78a) is arranged between said second (74c) and third (76) plane-like metal layers and said first and second transistors, formed in the semiconductor die (52).

As to claim 9, Eden et al., Figure 9, discloses an embodiment in which said second (111) and third (110) plane-like metal layers are arranged between said first plane-like metal layer (112) and said first and second transistors, in the semiconductor die (52a).

As to claim 10, Eden et al., Figure 7, discloses an insulating material, embodied as gaps, arranged between said first, second, third and fourth plane-like metal layers.

As to claim 24, Eden et al., Figure 14, discloses that the integrated circuit has a length to width ratio greater than 2:1.

As to claim 25, Eden et al., Figure 10 and paragraph [0089], discloses that the integrated circuit implements a power IC, said first contact portion, in column (144), supplies a first voltage potential (V_{DD}) to said power IC, said third contact portion supplies a second voltage potential (V_{SS}) to said power IC and said second contact portion receives an output voltage of said power IC.

As to claim 27, Eden et al., Figure 9, discloses an additional contact portion (118) that is arranged in said fourth plane-like metal layer, and local interconnects, embodied as bond pads (74d) and (132) (paragraph [0086]), that connect said additional contact portion with the control terminals (87) of said transistors.

As to claim 37, Eden et al., Figure 9, discloses that said first, second and third contact portions of said fourth plane-like metal layer (114a) substantially overlap an underlying area defined by said first and second transistors, in the semiconductor die (52a).

As to claim 38, Eden et al., Figure 9, discloses that the first, second and third contact portions cover the majority of the underlying area, which is within the scope of covering 1/3 of the underlying area.

As to claim 147, Eden et al., Figure 7, discloses that each of said first (78a), second (74c) and third (76) plane-like metal layers cover more than about 80% of both of said underlying transistors.

As to claim 148, Eden et al., Figure 7, discloses that said first plane-like metal layer (78a) covers greater than approximately 80% of both of said underlying first and second transistors and wherein said second (74c) and third (76) plane-like metal layers cover greater than approximately 80% of said first and second transistors, respectively.

As to claim 153, Eden et al., paragraph [0061], discloses that said first (78a), second (74c) and third (76) plane-like metal layers are planes, implicitely disclosing that current will flow in both x and y directions, where x is orthogonal to y.

Allowable Subject Matter

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention where said first transistor is a PMOS transistor, said second transistor is an NMOS transistor, said first and second control terminals are gates, said first terminal is a source, said second terminal is a drain, said third terminal is a drain, and said fourth terminal is a source.

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention wherein said first, second and third contact portions have an elliptical shape.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention wherein the first, second and third contact portions are generally rectangular and each cover about 1/3 of the underlying area defined by the first and second transistors, less an area between said first, second and third contact portions.

Claims 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention wherein said first and third contact portions have a base portion and wings that extend from said base portion, and wherein said second contact portions are received between said wings of said first and third contact portions.

Claims 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention wherein said first and third contact

portions have a base portion and wings that extend from said base portion, and wherein said second contact portions are received between said wings of said first and third contact portions.

Claims 17-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention wherein a first pair includes said first and second transistors and further comprising second, third and fourth pairs of transistors that are arranged in a generally square arrangement.

Claims 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with anything other than a circular shape for the contact portions.

Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention wherein said first contact portion supplies Vss to said first and second transistors, said second contract portion receives V_x from said first and second transistors and said third contact portion supplies V_{DD} to said first and second transistors.

Claims 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with first, second or third transmission lines communicating with first, second or third contact portions, respectively.

Claims 31-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with first, second or third transmission lines communicating with first, second or third contact portions, respectively.

Claims 39-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with third or fourth transistors connected

to the first and second, and first and third plane-like metal layers, respectively, or fourth and fifth contact portions in the fourth plane-like metal layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
November 13, 2006

LEONARDO ANDUJAR
PRIMARY EXAMINER